CLAIMS

1. A lateral bipolar CMOS integrated circuit comprising:

an inverter circuit comprising an n-channel MOS transistor and a p-channel MOS transistor, and having four terminals of:

a gate input terminal Vin connected with the gates of the n-channel MOS transistor and the p-channel MOS transistor;

an output terminal Vout connected with the drains of the n-channel MOS transistor and the p-channel MOS transistor;

a p-type base terminal connected with a p-type substrate of the n-channel MOS transistor; and

an n-type base terminal connected with an n-type substrate of the p-channel MOS transistor,

wherein the n-channel MOS transistor operates in a hybrid mode which is the hybrid of an operation mode of the MOS transistor and an operation mode of an npn lateral bipolar transistor which is inherent in the n-channel MOS transistor, and

the p-channel MOS transistor operates in a hybrid mode which is the hybrid of an operation mode of the MOS transistor and an operation mode of a pnp lateral bipolar

transistor which is inherent in the p-channel MOS transistor.

2. The lateral bipolar CMOS integrated circuit according to claim 1, wherein the gate input terminal Vin, the p-type base terminal and the n-type base terminal are input terminals of the inverter circuit, and the output terminal Vout is an output terminal of the inverter circuit, and

the inverter circuit outputs, at the output terminal Vout, a high-level or low-level voltage fed to the gate input terminal Vin as an inverted level voltage.

3. The lateral bipolar CMOS integrated circuit according to claim 2, comprising a current source Ibp connected with the p-type base terminal of the n-channel MOS transistor and a current source Ibn connected with the n-type base terminal of the p-channel MOS transistor,

wherein currents from the current source Ibp and the current source Ibn are maintained at 0 when the input voltage to the gate input terminal Vin is approximately constant at a high level or low level,

when the input voltage to the gate input terminal Vin switches from the low level to the high level, a forward pulse current flows from the current source Ibp to the p-

type base terminal in synchronization to switching, and

when the input voltage to the gate input terminal Vin switches from the high level to the low level, a forward pulse current flows from the current source Ibn to the n-type base terminal in synchronization to switching.

4. The lateral bipolar CMOS integrated circuit according to claim 3, further comprising a voltage source Vdd and a ground source Gnd,

wherein the current source Ibp is formed by a pull-up p-channel MOS transistor comprising a source terminal, a drain terminal and a substrate terminal, the drain terminal is connected with the p-type base terminal, and the source terminal and the substrate terminal are connected with the voltage source Vdd, and

the current source Ibn is formed by a pull-down n-channel MOS transistor comprising a source terminal, a drain terminal and a substrate terminal, the drain terminal is connected with the n-type base terminal, and the source terminal and the substrate terminal are connected with the ground source Gnd.

5. The lateral bipolar CMOS integrated circuit according to any one of claims 1 through 4,

wherein the inverter circuit comprising the n-channel

MOS transistor and the p-channel MOS transistor is used as a CMOS standard cell in the operation mode of the MOS transistor, but is used in the hybrid mode when a large load is connected with an output from the CMOS standard cell.